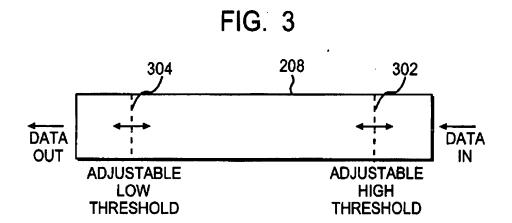
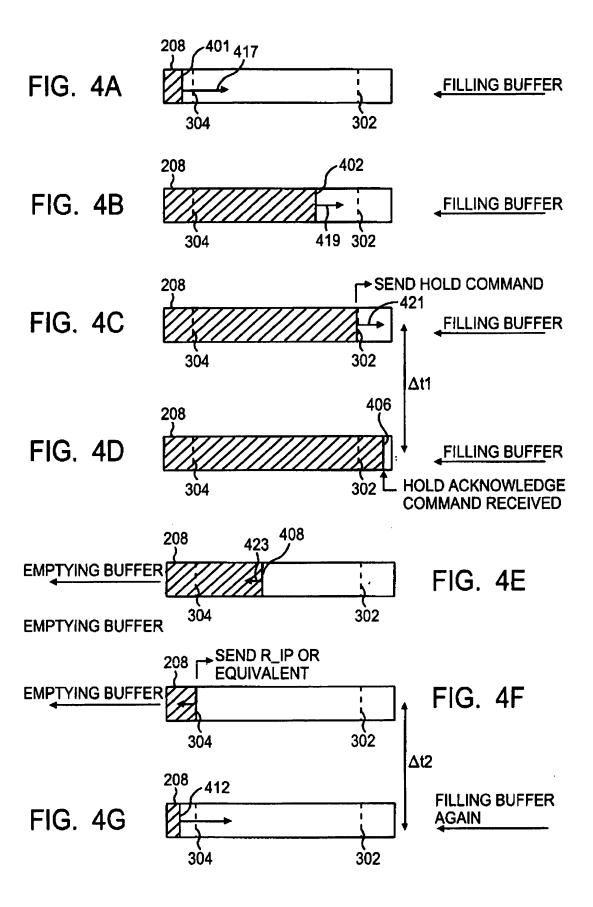


FIG. 2 140-150a 212 214 209 **PROCESSOR LINK LAYER** PHY **CIRCUITRY CIRCUITRY LAYER** 206 BUFFER CONTROL CIRCUITRY STP/SAS CONNECTION 210 208 **RECEIVE** DATA (**MEMORY** DATA **BUFFER** IN OUT 170 172





... ..

FIG. 5

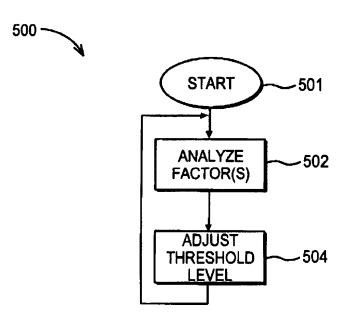
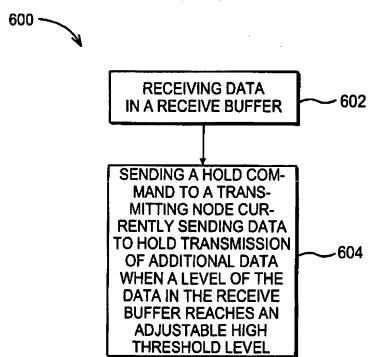


FIG. 6



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